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Diagnostic Access of AMBA-AHB Communication Protocols

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***Abstract*—In this paper a diagnostic access of AMBA AHB communication protocols is designed and implemented. AMBA AHB communication protocols are designed using master slave topology. A core is designed for implementation of communication protocols between master and slave device to perform efficient write operation. The process involves design and implementation of a master unit and a slave unit. Further a test bench is designed to simulate the communication between master and slave. A synthesis report of the process is generated using VHDL and XILINX. The process is configured for Address and Data bus of 32 bit width. The designed AMBA AHB communication protocol between master and single slave supports technology independent data transfer between high band width and high clock frequency multiprocessors and multi-CPU based embedded systems like arm processors and low bandwidth peripherals like IC based processors, standard macro cells, flash memory etc. The features required for high performance, high clock frequency systems including burst transfers, single clock edge operations, non–tristate implementation and wider data bus configuration are implemented in the design.**

***Index Terms*— AMBA (AHB), Communication protocols, Master-Slave topology, Core design, burst.**

I. INTRODUCTION [1]

During the last decade of the second millennium A.D, ARM was established. Within a few years, it took over the microcontroller market by introducing RISC architecture. It soon became a key component of the 32 bit embedded system and with this; there was a basic need for a new interfacing standard for bridging high performance ARM processors to low performance peripherals [1]. On chip communication standards for high performance embedded microcontrollers are defined in Advanced Microcontroller Bus Architecture (AMBA). [1].AMBA specification is well known for its extended bus standards. Among these, the most powerful is AHB(Advanced High Performance Bus).Here the interconnection process is designed in such a way that High performance and High clock frequency processors and other high bandwidth system cells can be efficiently interconnected[2].If High performance systems are to be connected, ASB(Advanced System Bus) is used[3]. The third standard is called APB (Advanced Peripheral Bus).When low bandwidth peripheral cells have to be connected to the main system, APB is used. This standard is also optimized for minimal

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power consumption and reduced complexity [3].

II. AMBA BASED INTERFACING [3]

High clock frequency high performance system bus (AHB) provides a backbone for bridging High memory bandwidth devices like multi-CPU multiprocessors based embedded systems like arm microcontrollers and direct memory access (DMA) devices to low bandwidth standard macro cells and peripheral devices supported by APB (AMBA Peripheral Bus) as shown in Figure 1. AMBA specification provides standard technology independent design standards and a roadmap for diagnostic accesses to test high performance microcontroller's connectivity to peripherals [6].

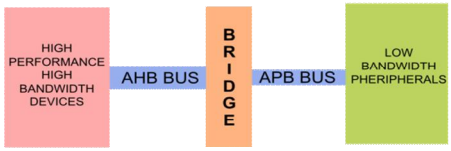

Figure 1.AHB to APB Bus

III. OPERATION OF CORE [3]

Figure 2 lists out all the signals which are made use of in the operation of the core. Initially master places a request signal and gets grant to start AMBA AHB transfer. When it is granted, the bus master drives address and control signals and starts the transfer process. Information regarding address, direction, width and if the transfer forms an incrementing or wrap burst are given by these address and control signals which are driven by the master. During the transfer if incrementing bursts are allowed, they do not wrap at the address boundaries whereas address gets incremented. If Wrapping bursts are selected they wrap at particular address boundaries. When master wishes to transfer the data to the slave write data bus is driven by the master. When slave wishes to transfer the data to master it drives read data bus. During each transfer an address bus is essential which is followed by one or more data cycles. Slaves are designed to sample the address during the process. To get extra time to sample the data slaves can include wait states into the transfer by asserting low on HREADY signal [6].

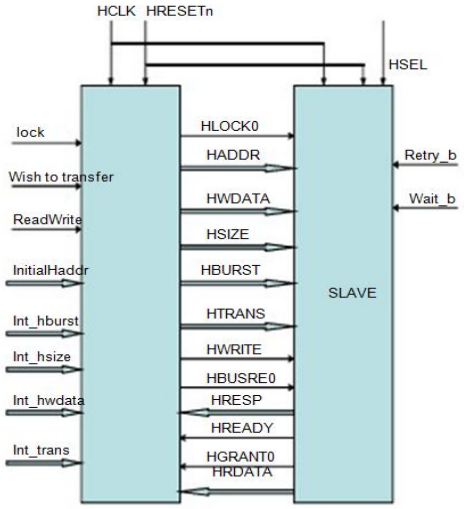

Figure 2.Block diagram of a core

A Response signal HRESP [1:0] indicates status of the slave transfer. There are 3 different HRESP [1:0] signals OKAY, ERROR and RETRY which indicate the status of transfer.

IV. LIST OF SIGNALS [3]

The following is the list of signals which are used in the operation of AMBA AHB processing. There are various signals which help in understanding the mode, transfer direction (towards or away from the slave), kind of data transfer (i.e. 4, 8 or 16 bit) etc.

- HCLK Bus clock: This signal gives clock times during raising edge related to all bus transfers.
- HRESET n RESET: When LOW HRESET resets the systems and the bus.
- HADDR [31:0]: Address bus: This refers to 32bit system address bus.
- HTRANS [1:0]: Transfer type: Whether current transfer is NONSEQUENTIAL, IDLE and BUSY transfer is indicated by HTRANS.
- HWRITE: Transfer Direction: It indicates write or read transfer when it goes HIGH or LOW respectively.
- HSIZE [2:0]: The size of the transfer is indicated by this signal. Typical sizes are BYTE (8 bit), half word or word (32 bit) exceeding even up to 1024bits.
- HBURST [2:0]: Burst type: This signal denotes if the transfer forms part of a four eight and sixteen beat bursts are supported and the burst may be either incrementing or wrapping.
- HWDATA [31:0] Write data bus: Data transfer from master to bus slave is obtained with HWDATA using write data bus. Data bus width extends from 32bits to higher range.

A. List Of Signals From Slave

- HSEL x Slave select: When a particular slave has to be selected for the current transfer it can be identified with its own select signal.
- HRDATA [31:0]: The data transfer from Read Data bus slaves to bus master during read operations is obtained with HRDATA [31:0]. Data bus width extends from 32 bits to higher bandwidth.
- HREADY transfer done: When transfer has finished on the HREADY signal indicates HIGH. To extend a transfer HREADY may be driven LOW.
- HRESP [1:0]: Transfer response additional information on the status of a transfer is indicated by HRESP. Four responses are included OKAY, ERROR, RETRY and SPLIT.

B. List Of Signals From Master To Slave

- HBUSREQ x: When bus master requires the bus it sends a request to the arbiter. Each bus master in the system is assigned with an HUSREQ x signal up to maximum of 16 bus masters.

C. Control Signals From Arbitter

- HGRANT x Bus grant: A particular bus master is currently assigned with highest priority by activating HGRANT x of a particular bus. A master gets access to the bus when both HREADY and HGRANT x are HIGH. When HREADY signal is HIGH at the end of a transfer ownership of the address/control signal changes.
- HMASTER [3:0] master number: Information about current transfer is indicated by HMASTER. This signal is used by slaves to perform SPLIT transfer and to determine about master which is attempting to access. The timing of HMASTER is properly matched with timing of address and control signals.
- HMASTLOCK Locked sequence: Whether the current master is performing a locked sequence of transfers this is indicated by locked sequence. This signal has same timing as that of HMASTER signal.
- HTRANS [1:0]: This signal indicates the state of transfer between the microcontroller and arbiter.

00 IDLE: When master is granted the bus but it does not wish to perform a data transfer. IDLE (00) indicates that no data transfer is required. During this slave provides a zero wait state OKAY response to IDLE transfers and ignore the transfer.

01 BUSY: When Bus masters are in the middle of burst of transfers they are allowed to place IDLE cycles by using BUSY transfer signal as 01.This indicates that the bus masters are busy in continuing with process of transfer of bursts and immediately next transfer cannot commence. Simultaneously address and control signals indicate the next transfer in the burst. Slave ignores the transfer as long as a master gives the BUSY

transfer type. During this slave provides a zero wait state OKAY response to IDLE transfers and ignore the transfer.
10 NONSEQ: First transfer is indicated by 10 NONSEQ signal. The address and control signals are independent of previous transfers.
11 SEQ: After the first transfer the remaining part of the burst transfer is SEQUENTIAL. During this transfer the address of the rest of transfers in a burst of transfers is dependent on previous transfer. The address is same as that of previous transfer added with size in bytes in case of incrementing burst. In wrapping burst wrapping of address of transfer takes place at the address boundary equal to size (in Bytes) which is multiplied by the number of beats (4, 8, or 16).The control information remains as in previous transfer.

V. BURST OPERATION [3]

In AMBA AHB four, eight, sixteen beat and undefined length bursts are well defined. Protocols support incrementing and wrapping bursts. Sequential locations are accessed by incrementing bursts. Address of each transfers increment of earlier address. In wrapping burst when boundary is reached the address of transfer the burst will wrap if start address of the transfers is not aligned to the total number of burst (size x beats).
There are eight modes of operation in Burst mode depending on the value of HBURST [2:0] [3].

- 000: SINGLE TYPE. This makes an indication that a single transfer is under progress.
- 001: INCR TYPE. This signal indicates an Increment burst of unspecified length.
- 010: WRAP 4TYPE. This signal indicates a 4 beat incrementing burst.
- 011: INCR 4TYPE. Indicates 4 beat incrementing burst.
- 100: WRAP 8TYPE. When an 8 beat wrapping burst is to be selected, this signal is activated.
- 101: INCR 8TYPE. This signal indicates 8 beat incrementing burst.
- 110: WRAP 16TYPE: This indicates a 16 beat wrapping burst.
- 111: INCR 16 TYPE: indicates 16 beat incrementing burst.

VI. ALGORITHM [6]

The following steps briefly demonstrate the various steps followed in the data transfer in AMBA AHB communication.

- Initially master places a request signal and gets grant to start AMBA AHB transfer after reset signal goes LOW.
- When the bus master is granted, it drives address and control signals and starts the transfer process when WISH TO TRANSFER signal goes high.
- Information regarding address, direction, width and if the transfer forms an incrementing or wrap burst are given by these address and control signals which are driven by the master.
- During transfer if incrementing bursts are allowed they do not wrap at the address boundaries whereas address gets incremented.
- During the transfer, if Wrapping bursts are selected they wrap at particular address boundaries.
- When master wishes to transfer the data to the slave write data bus is driven by the master.
- When slave wishes to transfer the data to master it drives read data bus.
- During each transfer an address bus is essential which is followed by one or more data cycles.
- Slaves are designed to sample the address during the process.
- To get Extra time to sample the data slaves can include wait states into the transfer by asserting low on HREADY signal.
- A Response signal HRESP [1:0] indicates status of the slave transfer. There are three different HRESP signals. They are OKAY asserted by slave which indicates normal progressing of data and also HREADY is driven high to indicate end of transfer, ERROR which is used to indicate that an error has occurred implying unsuccessful transfer and RETRY indicating that transfer is not complete.

VII. RESULTS

The simulation results are presented in Figure 3.

- ✓ INC8, 1Byte, no wait, no retry
- ✓ InitialHaddr

- ✓ <="00000000000000000000000000000110;
- ✓ int_hwdata <= int_hwdata+ 2 after 100 ns;
- ✓ int_hsize <= "000"; int_hburst <= "101";
- ✓ HRESETN <= '1','0' after 10 ns, '1' after 105 ns;
- ✓ Lock <= '0'; ReadWrite <= '1'; retry_B <= '0';
- ✓ HGRANT0<='1'; wait_B <= '0'; hsel <= '1

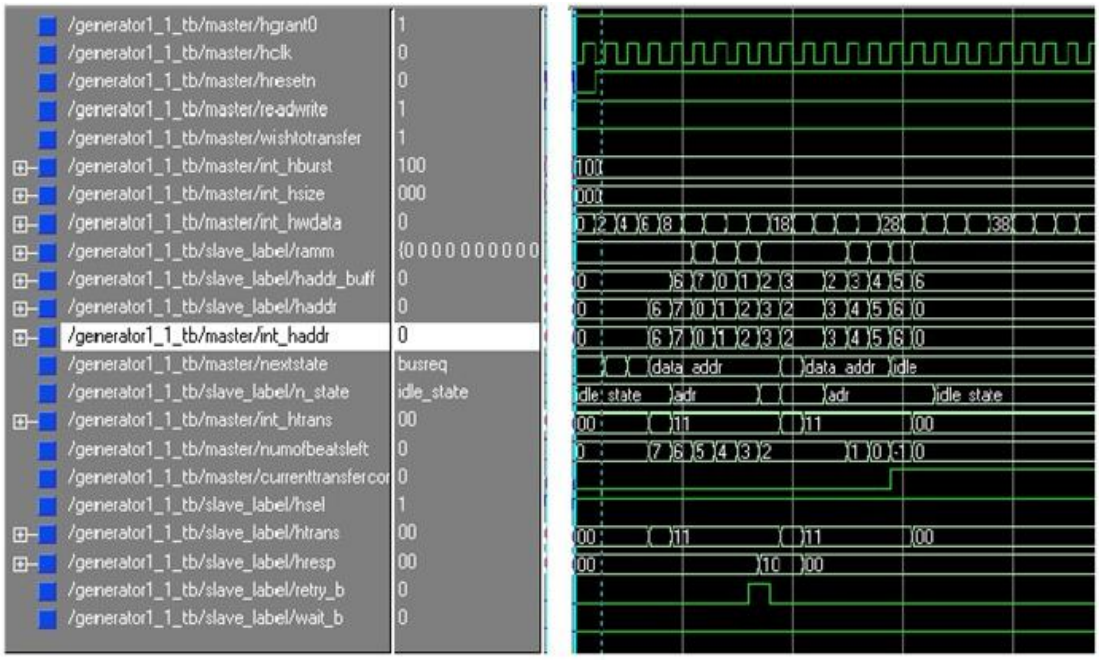

Figure 3.Simulation Results

VIII. ADVANTAGES OF AMBA AHB [5]

- This Protocol provides a good platform for development of multi CPU or multi signals processors based embedded microcontroller products with standard interfacing methods.
- This Technology independent protocol can be embedded for interconnecting diverse range of IC processors, reusable peripheral and system macro cells, and also digital units [2].
- AMBA AHB is useful in development of standard design for advanced cached CPU cores and peripheral libraries. They encourage independent modular system design [2].
- They minimize silicon usage and facilitates on chip and off chip communication for manufacturing test methods and operations [5].

IX. CONCLUSION

- A diagnostic access of AMBA AHB communication protocols is designed and implemented. AMBAAHB communication protocols are designed using master slave topology [3].
- A core is designed for implementation of communication protocols between master and slave device to perform efficient write operation. The process involves design and implementation of a master unit and a slave unit. A test bench is designed to simulate the communication between master and slave [6].
- A synthesis report of the process is generated using VHDL and XILINX. The process is configured for a 32 bit wide Address and Data bus [6].
- The designed AMBA AHB communication protocol between master and single slave supports technology independent data transfer between high band width and high clock frequency

multiprocessors and multi CPU based embedded systems like arm processors and low bandwidth peripherals like IC processors ,standard macro cells, flash memory etc[4].

- The features required for high performance, high clock frequency systems including burst transfers, single clock edge operations, non–tristate implementation and wider data bus configuration are implemented in the design[3].

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